PATENT
0465-0843P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	CHO, Dong Soo	Conf.:
Appl. No.:	NEW CONTINUATION APPLN. BASED ON 09/228,550	Group: Unassigned
Filed:	August 13, 2001	Examiner: Unassigned
For:	USER INITIATED MICRODE MODIFICATION	

PRELIMINARY RESPONSE

Assistant Commissioner for Patents
Washington, D.C. 20231

August 13, 2001

Sir:

Preliminary to examination of the above-identified application, the following remarks are submitted in connection with the above-identified application.

REMARKS

Claims 1-15 are pending. Claims 1, 3, 7, and 9 are independent claims.

These remarks correspond to those submitted on July 13, 2001 in the parent application (U.S. Serial No. 09/228,550).

Rejections based on Applicant's Admissions in view of Marlan et al.

Claims 1-8 (as numbered in the parent application) were rejected by the Examiner under 35 U.S.C. §103(a) over Applicant's Admissions in view of U.S.

Patent 5,829,012 to Marlan et al. (Marlan) for the reasons set forth in paragraphs 6-12 of the Final Office Action in the parent application dated April 13, 2001. Applicant respectfully traverses.

The Examiner, in the Final Office Action, acknowledges that Applicant's Admissions do not teach the claimed "user instruction selector," and relies upon Marlan to overcome this deficiency. Particularly, the Examiner asserts that the claimed user instruction selector reads on Marlan citing Abstract fig. 1, columns 1 and 2, col. 1 line 65 - col. 2, line 3, especially col. 1, line 66 - col 2. Line 3. The Applicant respectfully disagrees.

Marlan notes in col. 1 lines 24-34 the advantages and disadvantages of using a ROM for storing microcode, and seeks to overcome the disadvantages associated with the use of ROM by using RAM in conjunction with ROM. Specifically, Marlan teaches a mechanism for using a ROM and a RAM in combination to provide a single microcode address space allowing errant microcode to be corrected by replacing or adding new microcode (see Marlan col. 2 lines 6-65, especially lines 5-12). The storage of the corrected or new microcode in RAM is a necessary intervening step. Marlan also teaches remapping of a ROM to a RAM (See Marlan at col. 2, line 36, Fig. 3, and col. 6), further demonstrating that the use of RAM (with disadvantages) is essential to the practice of Marlan. Accordingly, Marlan does not disclose or suggest a user

instruction selector selecting or changing the micro-instructions from the micro-ROM in response to a selection by a user so as to change an operation of an instruction word corresponding to the instruction being fetched without any **subsequent intervening storage of the micro-instructions in RAM** (emphasis added).

The Examiner also maintains that Marlan teaches an "instruction code selector" according to Applicant's claim 3. Applicant respectfully disagrees. The Examiner cites the abstract, figs. 1 and 3, col. 7, lines 14-28 of Marlan. These applied references disclose devices that perform a variety of both data and address scanning operations ultimately directed to applying microcode patches. The process of replacing or adding new microcode employs an address RAM, a control store RAM, and an array of RAM addresses. It also employs a ROM remapping logic circuit, an array of ROM addresses, and a ROM. Further, the applied references of Marlan (Col 7, lines 14-28 and fig. 3) disclose that the operations required to replace or add microcode require a great number of address and data scans. Marlan discloses numerous devices performing a great number of operations but none that are directed to **encryption of instruction code**. Therefore Marlan does not disclose or suggest an instruction code selector, connected between the instruction register and the instruction decoder, allowing a user to select a signal corresponding to at least one of a

plurality of instruction maps wherein said instruction code selector is operable to **encrypt instruction code** (emphasis added).

The Examiner rejected claim 7 as having similar features as claims 1-6 and rejected them for the same reasons as cited in the rejections of claims 1-6. Applicant respectfully traverses examiner's rejection by asserting all arguments as to the patentability of claims 1-6.

In view of the above remarks, reconsideration and withdrawal of the rejections under 35 U.S.C. §103(a) based on AAPA in view of Marlan are respectfully requested.

Rejections of Claims 9-14 under 35 U.S.C. §102(e)

Claims 9-14 correspond to claims 9-14 of the parent application (added by the amendment of December 29, 2000) and have been rejected by the Examiner in the parent application under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 5,829,012 to Marlan et al. (Marlan) for the reasons set forth in paragraphs 13-22 of the Office Action. Applicant respectfully traverses.

Claim 9 presents claims similar to those presented in the preceding claims; therefore the arguments presented for allowance of the preceding claims are hereby incorporated by reference to support allowance of claim 9.

Applicant further points out that all other claims depend either directly or indirectly from either independent claims 1, 3, 7, or 9 and therefore are patentably distinguishable over Marlan or over AAPA in view of Marlan at least for the reasons discussed above.

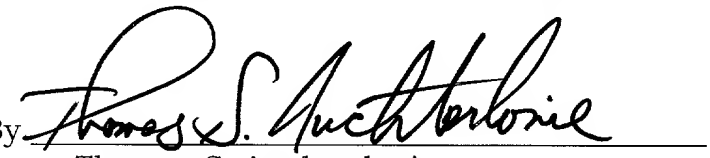
In view of the above remarks, reconsideration and withdrawal of the rejections under 35 U.S.C. §102 is respectfully requested.

In the event that any outstanding matters remain in this application, Applicant requests that the Examiner contact Thomas S. Auchterlonie (Reg. No. 37,275) at (703) 205-8071 to discuss such matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Very truly yours,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By 
Thomas S. Auchterlonie
Reg. No. 37,275

TSA/PLS/kmr

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000